PATENT

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Jan. 14, 2008 — Joanne Bourguignon

Date — Joanne Bourguignon

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Michael B. Raynham et al.
Application No.:	09/430,192
Filed:	October 29, 1999
Title:	Integrated Micro-Controller and Programmable Logic Device
Examiner:	Tonia L. Meonske
Art Unit:	2183
Docket No.:	10981963-1
Date:	January 14, 2007

Mail Stop Appeal Brief
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

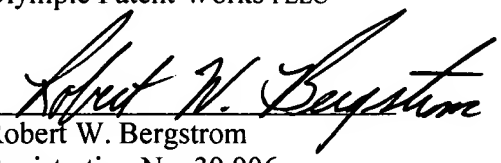
RESPONSE TO NOTIFICATION OF NON-COMPLIANT APPLEAL BRIEF UNDER 37 CFR § 41.37

Sir:

In response to the Appeal Brief filed September 6, 2007 and the Notification of Non-Compliant Appeal Brief under 37 CFR 41.37 dated December 12, 2007, Applicants respectfully submit an amended Appeal Brief that correctly contains a concise explanation of Claim 5 under the sections "grounds of rejection to be reviewed on appeal."

Applicant believes that no fee is required. However, at any time during the pendency of this application, please charge any fees required or credit any overpayment to Deposit Account No. 50-2976. A duplicate copy of this transmittal letter is enclosed.

Respectfully submitted,
Michael B. Raynham et al.
Olympic Patent Works PLLC



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Enclosures:

Postcards (2)
Amended Appeal Brief

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of:

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AMENDED BRIEF ON APPEAL

Commissioner of Patents and Trademarks
Washington, DC 20231

Sir:

This appeal is from the decision of the Examiner, in an Office Action mailed on February 15, 2007, finally rejecting claims 1-10.

REAL PARTY IN INTEREST

The real party in interest is Hewlett-Packard Development Company, LP, a limited partnership established under the laws of the State of Texas and having a principal place of business at 20555 S.H. 249 Houston, TX 77070, U.S.A. (hereinafter "HPDC"). HPDC is a Texas limited partnership and is a wholly-owned affiliate of Hewlett-Packard Company, a Delaware Corporation, headquartered in Palo Alto, CA. The general or managing partner of HPDC is HPQ Holdings, LLC.

RELATED APPEALS AND INTERFERENCES

Applicants' representative has not identified, and does not know of, any other appeals of interferences which will directly affect or be directly affected by or have a bearing

on the Board's decision in the pending appeal.

STATUS OF CLAIMS

Claims 1-10 are pending in the application. Claims 1-10 were finally rejected in the Office Action dated February 15, 2007. Applicants' appeal the final rejection of claims 1-10, which are copied in the attached Appendix.

STATUS OF AMENDMENTS

No Amendment After Final is enclosed with this brief. The last amendments to the claims were made in the Amendment filed November 21, 2006.

SUMMARY OF CLAIMED SUBJECT MATTER

Independent Claim 1

1. A subsystem controller (Current Application, page 1, lines 11-23; 712 and 718 in Figure 7; and 802 in Figure 8) implemented as a single integrated circuit (Current Application, page 4, line 27) for control of a device (318, 320-323 in Figure 3) or subsystem (716 in Figure 7) within an electronic system (702, 704, 706, 708, 710, 712, 714, 716, 718, 722 in Figure 7) having system processing components (702 in Figure 7), the subsystem controller comprising:

a complex programmable logic device (804) that can be programmed to provide logic circuits that implement control functionality (Current Application, page 6, lines 14-15);

a micro-controller (806) that can execute software routines that implement control functionality (Current Application, page 6, lines 15-16);

read-only memory (808) that stores executable code for execution by the micro-controller (Current Application, page 5, lines 11-14);

random-access memory (810) that can store data and executable code for execution by the micro-controller (Current Application, page 5, lines 11-14);

a bus interface (812-815) for exchanging data and control signals between the subsystem controller and system processing components; and

an additional electronic interface (816-817) to a device or subsystem controlled by the subsystem controller (Current Application, page 9, lines 22-25).

Dependent Claims 2-5

2. The subsystem controller of claim 1 wherein control functionality of the subsystem controller is partitioned between logic circuits programmed into the complex programmable logic device and software routines executed by the micro-controller (Current Application, page 5, lines 7-11; Figure 2; and Current Application, page 6, line 20 - page 7, line 11).

3. The subsystem controller of claim 1 programmed to control display of information on a liquid-crystal display window (318) included in an external front panel (302) display of a server computer.

4. The subsystem controller of claim 1 wherein the bus interface is an inter-integrated circuit bus interface (816-817).

5. The subsystem controller of claim 1 wherein the additional electronic interface is an 8-bit input/output bus and additional signal lines (Current Application, page 9, lines 22-25).

Independent Claim 6

6. A method for controlling a subsystem (716 in Figure 7) within a complex electrical device (702, 704, 706, 708, 710, 712, 714, 716, 718, 722 in Figure 7), the method comprising:

providing a single-integrated-circuit subsystem controller (Current Application, page 1, lines 11-23; 712 and 718 in Figure 7; 802 in Figure 8; and page 4, line 27);

programming control functionality into the single-integrated-circuit subsystem controller by

programming logic circuits into a complex programmable logic device included in the single-integrated-circuit subsystem controller (Current Application, page 5, lines 7-11; Figure 2; and Current Application, page 6, line 20 - page 7, line 11),

implementing software routines for execution by a micro-controller within the single-integrated-circuit controller (Current Application, page 5, lines 7-11; Figure 2; and

Current Application, page 6, line 20 - page 7, line 11), and

storing the software routines in the single-integrated-circuit subsystem controller (Current Application, page 5, lines 11-14); and

interconnecting the single-integrated-circuit subsystem controller to the subsystem within the complex electrical device (Current Application, page 9, lines 22-25).

Dependent Claims 7-10

7. The method of claim 6 wherein the subsystem is a liquid-crystal display window (318) that displays information about the components within the complex electrical device and about the state of the complex electrical device.

8. The method of claim 6 wherein the complex electrical device is a computer system (702, 704, 706, 708, 710, 712, 714, 716, 718, 722 in Figure 7).

9. The method of claim 6 wherein the single-integrated-circuit subsystem controller includes the complex programmable logic device(804), the micro-controller (806), a read-only memory (808), a random-access memory (810), a bus interface (12-815), and an additional electronic interface (816-817).

10. The method of claim 9 wherein interconnecting the single-integrated-circuit subsystem controller to the subsystem within the complex electrical device further includes interconnecting the subsystem with the additional electronic interface (Current Application, page 9, lines 22-25).

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. The rejection of claims 1, 2, 4, 6, 8, 9, and 10 under 35 U.S.C. § 102(b) as being clearly anticipated by Uming U-Ming Ko, European Patent Application 0 419 105 A2 ("Ko").

2. The rejection of claims 3 and 7 under 35 U.S.C. § 103(a) as being unpatentable over Ko in view of Alexander, U.S. Patent No. 5,953,684 ("Alexander").

3. The rejection of claim 5 under 35 U.S.C. § 103(a) as being unpatentable over Ko.

ARGUMENT

Claims 1-10 are pending in the current application. After initially responding to four office actions, in which the claims of the current application were rejected over completely unrelated references, Appellants filed an Appeal Brief, on June 4, 2004. In response to the Appeal Brief, the Examiner reopened prosecution with an office action dated August 22, 2006. In an office action dated February 15, 2007 ("Office Action"), the Examiner finally rejected claims 1, 2, 4, 6, 8, 9, and 10 under 35 U.S.C. § 102(b) as being clearly anticipated by Uming U-Ming Ko, European Patent Application 0 419 105 A2 ("Ko"), finally rejected claims 3 and 7 under 35 U.S.C. § 103(a) as being unpatentable over Ko in view of Alexander, U.S. Patent No. 5,953,684 ("Alexander"), and finally rejected claim 5 under 35 U.S.C. § 103(a) as being unpatentable over Ko. Appellants then filed an Appeal Brief, on September 6, 2007, which the Examiner correctly found to be lacking a clear indication of traversal of the rejection of claim 5, in an office communication dated December 12, 2007. Appellants therefore file the current, Amended Appeal Brief, in which Appellants respectfully traverse the final 35 U.S.C. § 102(b) and 35 U.S.C. § 103(a) rejections included inn the Office Action.

ISSUE 1

1. The rejection of claims 1, 2, 4, 6, 8, 9, and 10 under 35 U.S.C. § 102(b) as being clearly anticipated by Ko.

Claim 1 is representative of the rejected claims, and is provided below, with emphasis added, to facilitate the following discussion:

> 1. A **subsystem controller** implemented as a single integrated circuit **for control of a device or subsystem within an electronic system** having system processing components, the **subsystem controller** comprising:
>
> **a complex programmable logic device that can be programmed to provide logic circuits that implement control functionality;**
>
> **a micro-controller that can execute software routines that implement control functionality;**
>
> read-only memory that stores executable code for execution by the micro-controller;

random-access memory that can store data and executable code for execution by the micro-controller;

a bus interface for exchanging data and control signals between the subsystem controller and **system processing components**; and

an additional electronic interface to a device or subsystem controlled by the subsystem controller.

The bolded portions of claim 1, above, indicate claim language neither disclosed, taught, or suggested by Ko.

The phrase "subsystem controller" is well known to those familiar with modern computer systems, and subsystem controllers are described, in the first paragraph of the current application, as follows:

> Subsystem controllers are ubiquitous components of modern computer systems, peripheral devices within computer systems, and other electronic devices. The term "subsystem controller" generally refers to a subcomponent of a more complex electronic system, such as a computer, that comprises logic circuits, a programmable logic device, and a general-purpose micro-controller that executes a number of software routines. A subsystem controller is generally dedicated to one or a small number of specific control tasks. For example, the control of LED and LCD display devices incorporated in a front panel display of a computer system is generally carried out by one or more subsystem controllers. Use of subsystem controllers may offload computationally intensive and time-intensive tasks from the main processor or processors of computer systems, and may significantly decrease data traffic on critical busses of the computer system that are bottlenecks for data movement within the computer system.

The current application describes one, exemplary subsystem controller 802, shown as a block diagram, in Figure 8, that controls an LCD display 318 included on the front panel 302 of a computer server. This exemplary subsystem controller can be appreciated to exemplify subsystem controllers as described in the above paragraph, and as clearly claimed in claim 1. The exemplary subsystem controller is "dedicated to one or a small number of specific control tasks." The exemplary subsystem controller offloads "computationally intensive and time-intensive tasks from the main processor or processors" of the server computer, "and may significantly decrease data traffic on critical busses" of the server computer "that are bottlenecks for data movement within the" server computer. The exemplary subsystem controller is "implemented as a single integrated circuit for control of a device or subsystem within an electronic system having system processing components," includes "a bus interface for exchanging data and control signals between the subsystem controller and system processing components," and includes "an additional electronic interface to a device or

subsystem controlled by the subsystem controller," as clearly claimed in claim 1.

The current application and claims are directed to a novel subsystem controller and method for controlling a subsystem within a complex electrical device, in which the subsystem controller is implemented using both a complex programmable logic device ("CPLD"), such as a programmable logic array, and a micro-controller, with controller functionality partitioned between the CPLD and micro-controller. As stated in the current application on line 20 of page 6 to line 11 of page 7:

> Figure 2 graphically illustrates the flexibility in partitioning control functionality between hardware and software in the single-IC subsystem controller device that represents one embodiment of the present invention. Figure 2 is nearly identical to Figure 1, with exception that the fixed arrow (100 in Figure 1) has been replaced by a slidable partition 202. Using the single-IC subsystem controller device of the present invention, *the manufacturer of various subsystem controllers can choose arbitrary partitionings of control functionality between hardware and software. Thus, the partitioning is not fixed, as in previous subsystem controllers, but is flexible. The flexibility arises from the ability to program both the CPLD and the micro-controller in the single-IC subsystem device.* For example, in an application where only extremely efficient, low-level logic functional control is needed, the entire control functionality may be implemented by programming the CPLD of the single-IC subsystem controller device. In such an application, there is no need for executing software routines on the micro-controller. For another application in which only high-level, complex logic is required, and there is little or no requirement for time-critical and time-intensive interfacing to an electric device at the circuit level, the entire control functionality may be implemented as a collection of software routines stored in the EEPROM or downloaded into the SRAM and executed by the micro-controller. I*n between the two extremes are an almost limitless number of different control functionality partitionings between hardware and software available to the subsystem controller designer and manufacturer of the single-IC subsystem controller device.* (emphasis added)

Thus, using both the CPLD and micro-controller allows for a flexible approach to subsystem controller implementation, allowing a wide variety of different subsystem controllers to be implemented using a single integrated circuit.

Ko does not disclose, teach, mention, or suggest a subsystem controller. Applicants' representative cannot find a single instance of the phrase "subsystem controller" in Ko, nor a single instance of any synonymous phrase or term. Instead, as stated explicitly by Ko on lines 11-18 of column 7, Ko is directed to an integrated circuit that comprises a digital signal processor circuit formed on a portion of a semiconductor substrate, the remaining portion of which is used to construct additional circuits which are useful in specific

applications to interface the digital signal processor core with other components of an integrated data processing system. As is clear to those familiar with computer science and computer systems, digital signal processors are high-end processing devices used, as the name "digital signal processor" ("DSP") suggests, for computational signal processing. Applicants' representative can think of no case in which a high-bandwidth, complex, and expensive DSP would be used as, or incorporated in, a subsystem controller. As discussed in the paragraph on lines 14-24 of page 4 of the current application:

> Designers and manufacturers of subsystem controllers have therefore recognized a need for a *versatile, low-cost, easily programmable, and energy-efficient subsystem controller device that can be programmed for a variety of different applications*. A versatile subsystem controller device could be manufactured in high volume, thus decreasing design and implementation costs associated with low-volume single-application subsystem controllers. Furthermore, a versatile, easily programmable subsystem controller devices would allow for hardware standardization and decreased overall system design costs, while still allowing manufacturers to include proprietary control functionality within the subsystem controller device via proprietary programmable logic device programming and via proprietary software routines for execution on a micro-controller.

Thus, subsystem controllers need to be "versatile, low-cost, easily programmable, and energy-efficient," essentially low-cost controllers for specific control tasks within a computer system. DSPs are clearly not subsystems controllers, being instead designed for use in processing digital signals obtained by analog-to-digital conversion, as described by the Wikipedia entry for digital signal processors:

> A **digital signal processor (DSP)** is a specialized microprocessor designed specifically for digital signal processing, generally in real-time computing.
>
> Characteristics of typical Digital Signal Processors
>
> - Designed for real-time processing
> - Optimum performance with streaming data
> - Separate program and data memories (Harvard architecture)
> - Special Instructions for SIMD (Single Instruction, Multiple Data) operations
> - No hardware support for multitasking
> - The ability to act as a direct memory access device if in a host environment
> - Processes digital signals converted (using an Analog-to-digital converter (ADC)) from analog signals. Output is then converted back to analog form using a Digital-to-analog converter (DAC)

In rejecting claim 1, the Examiner points to Figure 1 of Ko as teaching a subsystem controller, in section 3 of the Office Action. As clearly claimed in claim 1, the subsystem controller to which the present invention is directed controls another device or subsystem. Ko does not teach, mention, or suggest control of another device or subsystem by Ko's DSP. That is unsurprising, given that DSPs are not designed for, or used as, subsystem controllers for controlling devices and/or subsystems. Referencing a single figure that depicts a DSP integrated circuit, unrelated to a subsystem controller, falls far short of the requirement for a *prima facie* anticipation rejection - namely that the anticipating reference teach every element of the claim. Please note that Ko does not once state or suggest that Ko's single-IC DSP is a subsystem controller. Instead, the Examiner appears to have decided to redefine the well-known phrase "subsystem controller" to an arbitrary definition that would encompass both subsystem controllers and DSPs. That arbitrary redefinition is not supported by any reference, dictionary definition, or even a vague reference to any definition known to those skilled in the art. A DSP is simply not a subsystem controller. Of course, an Examiner must give the broadest reasonable interpretation to a claim. But interpreting the well-known phrase "subsystem controller," clearly described in the current application, to read on a DSP is not a reasonable interpretation, in light of how the phrase is understood in the art and in light of the specification.

In rejecting the first element of claim 1, the Examiner cites element 38 of Figure 1 and line 22 of column 4 of Ko. The full cited sentence reads: "For example, the user-definable circuitry area 24 could be used to form a bus-controller circuit 34, an I/O driver circuit or a programmable logic array (PLA) 38." This citation falls far short of a teaching of "a complex programmable logic device that can be programmed to provide logic circuits that implement control functionality." Ko does not teach, mention, or even suggest implementing any kind of control functionality in PLA 38. Moreover, the phrase "control functionality" in claim 1 is not an arbitrary phrase that can be interpreted in any fashion that meets the Examiner's purpose. Claim 1 is directed to a "subsystem controller implemented as a single integrated circuit for control of a device or subsystem within an electronic system" that includes "an additional electronic interface to a device or subsystem controlled by the subsystem controller." The word "control" in claim 1 refers to "control of a device or subsystem." There is nothing in Ko that suggests that PLA 38 is implemented to, or capable of, control any kind of device or subsystem. There is no teaching, suggestion, or mention of a connection between the PLA and pins, bus interfaces, or any other communications

medium that would interconnect the PLA to an external device or subsystem, or even other internals components of Ko's DSP. Instead, the only reference to the PLA 38 is four words and a parenthesized acronym at the end of the above quoted sentence.

In rejecting the second element of claim 1, the Examiner cites line 55 of column 1 to line 6 of column 2, lines 49-50 of column 2, and element 12 of Figure 1. The passage occurring on line 55 of column 1 to line 6 of column 2 discusses the "remainder of the semiconductor substrate ... available for additional peripheral circuitry to implement necessary circuitry to allow the digital signal processor to perform complex microcontroller and other applications without the degradation in speed associated with systems requiring interchip communications." By "remainder," Ko means that portion of the monolithic integrated circuit that does not include the embedded digital signal processor, as explicitly stated by Ko on lines 51-55. The cited sentence of column 2 reads: "A digital signal processor 12 is formed on a portion of the surface area of chip 10." Thus, the Examiner is citing the entire monolithic integrated circuit shown in Figure 1 of Ko, including the user-definable circuitry in portion 24 (*see* column 4, lines 28-31) and the embedded digital signal processor 12. This rejection makes absolutely no sense. As discussed above, and discussed further below, a monolithic-integrated-circuit implementation of a digital signal processor is not a subsystem controller. The second element of claim 1 reads: "a micro-controller that can execute software routines that implement control functionality." A DSP implementation that includes a DSP and a RAM, ROM, bus controller, I/O driver, and PLA separate from the DSP, is not a microcontroller. For example, the Wikipedia entry for microcontroller reads, in part:

> A **microcontroller** (or **MCU**) is a computer-on-a-chip. It is a type of microprocessor emphasizing self-sufficiency and cost-effectiveness, in contrast to a general-purpose microprocessor (the kind used in a PC). The only difference between a microcontroller and a microprocessor is that a microprocessor has three parts - ALU, Control Unit and registers (like memory), but the microcontroller has additional elements like ROM, RAM etc.
>
> Embedded design
>
> The majority of computer systems in use today are embedded in other machinery, such as telephones, clocks, appliances, vehicles, and infrastructure. An embedded system usually has minimal requirements for memory and program length and may require simple but unusual input/output systems. For example, most embedded systems lack keyboards, screens, disks, printers, or other recognizable I/O devices of a personal computer. They may control electric motors, relays or voltages, and read switches, variable

> resistors or other electronic devices. Often, the only I/O device readable by a human is a single light-emitting diode, and severe cost or power constraints can even eliminate that.
>
> Higher Integration
>
> In contrast to general-purpose CPUs, microcontrollers may not implement an external address or data bus, because they integrate RAM and non-volatile memory on the same chip as the CPU. Because they need fewer pins, the chip can be placed in a much smaller, cheaper package.

However, Ko's monolithic implementation of a DSP includes: an embedded DSP (12) that, in turn, includes a ROM (14), a multiplier circuit (22), RAM 16, and an ALU (20); RAM (30), ROM (32), a bus controller (34), and I/O driver (36); and a PLA (38). Moreover, Ko's monolithic implementation of a DSP includes 216 universal 1/O bond pads - hardly the small package with a minimal number of pins discussed in the Wikipedia entry. Ko's monolithic implementation of a DSP is not a microcontroller - and no one familiar with computer systems and integrated circuits would suggest that Ko's monolithic implementation of a DSP is a microcontroller.

Later, in section 18 of the Office Action, the Examiner states: "Element 12 executes microprograms (or software routines), which are stored in ROM, to control and manipulate data (column 2, lines 51-54). Therefore, the digital signal processor of KO, element 12, is capable of executing software routines that implement control functionality ... i.e. control the manipulation of data." In this section of the Office Action, by contrast to the rejection of claim 1 in section 3, the Examiner appears to consider the embedded digital signal processor (12 in Figure 1 of Ko) to be a microcontroller. However, it is apparent that the Examiner is trying very hard to read claim language directed to a subsystem controller onto an unrelated device.

The phrase used by the Examiner, "controlling the manipulation of data," is not used in Ko, and appears to have no apparent meaning, other than an attempt to redefine claim language to allow claim 1 to be read onto Ko's DSP implementation. The argument used to try to fit Ko's embedded DSP to "a micro-controller that can execute software routines that implement control functionality" ignores basic principles of claim interpretation and the explicitly stated, quite transparent essence of the present invention. As discussed above, the word "control" in claim 1 refers to control of a device or subsystem, and DSPs are not designed for, and not used for, control of devices or subsystems. Ko does not once suggest such a use for Ko's embedded DSP. There is, in the current application and, in

particular, in claim 1, no meaning associated with the word "control" other than control of a device or subsystem,. Applicants are not disclosing and claiming a *data* controller or DSP, but are clearly and unambiguously disclosing and claiming a subsystem controller.

As discussed above, the present invention is directed to a subsystem controller implementation in which control functionality is partitioned between a CPLD and a microcontroller. In claim, the same phrase "control functionality" is used in both the first element, directed to the CPLD, and the second element, directed to the microcontroller," to reflect the above-discussed partitioning of control functionality between the CPLD and the microcontroller. The phrase refers to control of a device or subsystem, as clearly claimed in claim 1 and as abundantly clear from the above-quoted passages of the current application. By contrast, the Examiner has attempted to redefine "control" to mean "control of data manipulation" in order to read "a micro-controller that can execute software routines that implement control functionality" onto an embedded DSP. However, the Examiner has failed to point to any kind of control functionality associated with PLA 38. There is no teaching, mention, or suggestion in Ko that the PLA 38 is also used to "control the manipulation of data," whatever that phrase means, and no teaching or suggestion that PLA 38 is used or intended to be used to "control the manipulation" or the same data manipulated by the embedded DSP. There is no suggestion in Ko that DSP "control of data manipulation" is carried out by any other entity within Ko's DSP implementation. By contrast, there are many suggestions in Ko that the peripheral circuitry implemented in the non-DSP portion of Ko's monolithic integrated circuit is devoted to interchip communications (*see* line 55 of column 1 to line 11 of column 2 and lines 15 - 27 of column 4). Thus, had the Examiner pointed to a meaning for the phrase "control functionality" in the rejection of the first element of claim 1, it would most certainly have been a different "control functionality" than that of the "control of data manipulation" attributed by the Examiner to the embedded DSP of Ko. Claim 1 does not use phrases "first control functionality" and "second control functionality." Instead, claim 1 employs the same phrase "control functionality" deliberately to indicate that control functionality is partitioned between the microcontroller and the CPLD, and that control functionality is control of a device or subsystem controller, the well-known function of a subsystem controller. Ko does not teach, mention, or suggest any common functionality shared by the embedded DSP and PLA 38, let alone a common "control functionality."

For the third and fourth elements of claim 1, the Examiner cites the ROM (14) and RAM (16) components of the DSP. Again, the rejections make no sense. Claim 1 claims

a microcontroller as a separate element from the RAM and ROM claimed in the third and fourth elements of claim 1, rather than claiming the RAM and ROM as components of the microcontroller claimed in the second element of claim 1. However, Figure 1 of Ko does show a RAM (30) and a ROM (32) external to the embedded DSP.

The Examiner cites "[a]ny combination of elements 26, 34, and 28 as the bus interface claimed by the fifth element of claim 1 "a bus interface for exchanging data and control signals between the subsystem controller and system processing components." Again, the rejection makes no sense. Elements 26, 34, and 28 are explicitly stated by Ko to be: (1) parallel module testing multiplexers 26 that interface the embedded DSP with the user-defined circuitry of Ko's monolithic IC (see column 3, lines 49-52); (2) a bus controller circuit 34; and (3) universal I/O bond pads that interconnect Ko's monolithic IC with other components of a data processing system. There is no indication in Ko that the bus controller is in any way associated with the I/O controller. I/O controllers are generally devoted to control of peripheral devices, and not to system processing components. The parallel module testing multiplexers interconnect the embedded DSP with other portions of Ko's monolithic IC, rather than to system processing components external to the monolithic IC. Thus, the fifth element of claim 1 can only possibly be read on the bus controller of Ko. The other entities mentioned by the Examiner do not constitute "a bus interface for exchanging data and control signals between the subsystem controller and system processing components." Even in the case of the bus controller, Ko does not appear to state that the bus controller interfaces the DSP to a system *processing* component, but only that it may facilitate interconnection of the embedded DSP with other system components.

The Examiner again cites universal I/O bond pads 28 as teaching the sixth element of claim 1: "an additional electronic interface to a device or subsystem controlled by the subsystem controller." However, Ko does not once teach, mention, or suggest that Ko's DSP controls any kind of device or subsystem via universal I/O bond pads 28. Instead, Ko explicitly states that the universal I/O bond pads 28 are used for communications between Ko's monolithic IC and other components of an integrated data processing system, on lines 53-56 of column 3. Later, Ko discusses a test interface partially implemented using the universal I/O bond pads 28. However, the test interface is an interface that allows an external processor to test the DSP, and has nothing whatsoever to do with control of a device or subsystem by the DSP. Furthermore, the sixth element of claim 1 is distinct from the fifth element. Basic principles of claim interpretation would seem to prohibit reading two distinct

elements of a claim onto a single component of device, especially when one of the elements is prefaced by the phrase "an additional electronic interface."

In summary, the Examiner has failed to find a teaching or disclosure of the first, second, and sixth elements of claim 1, and has failed to point to any device disclosed in Ko that can possibly be interpreted as a subsystem controller. A DSP is a digital signal processor, and is designed and used to carry out various mathematical transformations of digital signals. It is not a subsystem controller. A complex single-IC implementation of a DSP is not an inexpensive, low-power device dedicated to one or a small number of specific device-control or subsystem-control tasks within a computer system. Nothing in Ko teaches, mentions, or suggests partitioning device-control or subsystem-control functionality between a CPLD and a microcontroller within a subsystem controller, or a microcontroller and CPLD that both implement and/or execute control functionality.

Independent claim 6 includes much language similar or identical to that of claim 1. For example, independent claim 6 is directed to a "method for controlling a subsystem within a complex electrical device," in which "control functionality" is both programmed into a complex programmable logic device and implemented as software routines executed by a micro-controller. For the same reasons that Ko is unrelated to the subsystem controller to which claim 1 is directed, Ko is unrelated to the method of claim 6. None of the claims that depend from independent claims 1 and 6 are anticipated by Ko, since independent claims 1 and 6 are not anticipated by Ko.

ISSUE 2

2. The rejection of claims 3 and 7 under 35 U.S.C. § 103(a) as being unpatentable over Ko in view of Alexander.

Both the rejection of claim 3 and claim 7, in section 11 of the Office Action, depend on the assumption that Ko teaches the subsystem controller of claim 1 and the method of claim 6. As discussed above, Ko does not teach, mention, or disclose a subsystem controller or the method for controlling a subsystem within a complex electrical device as claimed in claim 6. As discussed in MPEP § 2143, a combination of references must teach every claim element, and, as discussed above, Ko does not teach, mention, or suggest a subsystem controller, and, in particular, fails completely to teach, mention, or suggest a subsystem controller in which control functionality is partitioned between a microcontroller

and a CPLD. Therefore, the rejections of claims 3 and 7 necessarily fail for the same reason that the above-discussed rejections of claims 1, 2, 4, 6, 8, 9, and 10 under 35 U.S.C. § 102(b) fail.

ISSUE 3

3. The rejection of claim 5 under 35 U.S.C. § 103(a) as being unpatentable over Ko.

The rejection of claim 5, in section 14 of the Office Action, depends on the assumption that Ko teaches the subsystem controller of claim 1. As discussed above, Ko does not teach, mention, or disclose a subsystem controller. As discussed in MPEP § 2143, a reference or combination of references must teach every claim element, and, as discussed above, Ko does not teach, mention, or suggest a subsystem controller, and, in particular, fails completely to teach, mention, or suggest a subsystem controller in which control functionality is partitioned between a microcontroller and a CPLD. Therefore, the rejection of claims 5 necessarily fails for the same reason that the above-discussed rejections of claims 1, 2, 4, 6, 8, 9, and 10 under 35 U.S.C. § 102(b) fail.

CONCLUSION

The current application was filed in October of 1999. In a series of Office Actions, from April of 2002 until November of 2003, the Examiner asserted and maintained rejections of the current claims based on completely unrelated references. After Applicants appealed these rejections, in March of 2004, the Examiner abandoned the initial rejections, based on the completely unrelated references, and reopened prosecution to assert the current rejections that, as discussed above, fall short of meeting the requirements of *prima facie* anticipation and obviousness-type rejections. The current claims are directed to a subsystem controller that controls an external device or subsystem, and in which control functionality is partitioned between a CPLD and a microprocessor. By contrast, Ko discloses a DSP. A DSP is not a subsystem controller, and is not used to control either a device or a subsystem within a computer system in order to offload processing load from one or more CPUs and to decrease communications overhead within the computer system. DSPs are, by contrast, used for digital signal processing, as the name "digital signal processor" implies. There is no mention in Ko of partitioning control functionality between a CPLD and a microcontroller.

Ko is completely unrelated to the currently claimed invention. The fact that the Examiner has failed to find a teaching or suggestion for many claim limitations of the current claims in Ko, which discloses a DSP, rather than a subsystem controller, is quite unsurprising, in view of the significant differences between DSPs and subsystem controllers. In Applicants' representative's respectfully offered opinion, eight years of prosecution of a relatively straightforward application, including six office actions and two appeal briefs, represents and unwarranted and unfair burden on Applicants, particularly in view of the fact that the Examiner has yet to cite a single relevant reference. Applicants' representative believes that the failure of the Examiner to find a reference or combination of references that teach or suggest all of the claim limitations of the current claims during the course of eight years is very strong evidence that the current claims are directed to a novel and non-obvious device and method.

Applicant respectfully submits that all statutory requirements are met and that the present application is allowable over all the references of record. Therefore, Applicant respectfully requests that the present application be passed to issue.

Respectfully submitted,
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APPENDIX

1. A subsystem controller implemented as a single integrated circuit for control of a device or subsystem within an electronic system having system processing components, the subsystem controller comprising:

a complex programmable logic device that can be programmed to provide logic circuits that implement control functionality;

a micro-controller that can execute software routines that implement control functionality;

read-only memory that stores executable code for execution by the micro-controller;

random-access memory that can store data and executable code for execution by the micro-controller;

a bus interface for exchanging data and control signals between the subsystem controller and system processing components; and

an additional electronic interface to a device or subsystem controlled by the subsystem controller.

2. The subsystem controller of claim 1 wherein control functionality of the subsystem controller is partitioned between logic circuits programmed into the complex programmable logic device and software routines executed by the micro-controller.

3. The subsystem controller of claim 1 programmed to control display of information on a liquid-crystal display window included in an external front panel display of a server computer.

4. The subsystem controller of claim 1 wherein the bus interface is an inter-integrated circuit bus interface.

5. The subsystem controller of claim 1 wherein the additional electronic interface is an 8-bit input/output bus and additional signal lines.

6. A method for controlling a subsystem within a complex electrical device, the method comprising:

providing a single-integrated-circuit subsystem controller;

programming control functionality into the single-integrated-circuit subsystem controller by

programming logic circuits into a complex programmable logic device included in the single-integrated-circuit subsystem controller,

implementing software routines for execution by a micro-controller within the single-integrated-circuit controller, and

storing the software routines in the single-integrated-circuit subsystem controller; and

interconnecting the single-integrated-circuit subsystem controller to the subsystem within the complex electrical device.

7. The method of claim 6 wherein the subsystem is a liquid-crystal display window that displays information about the components within the complex electrical device and about the state of the complex electrical device.

8. The method of claim 6 wherein the complex electrical device is a computer system.

9. The method of claim 6 wherein the single-integrated-circuit subsystem controller includes the complex programmable logic device, the micro-controller, a read-only memory, a random-access memory, a bus interface, and an additional electronic interface.

10. The method of claim 9 wherein interconnecting the single-integrated-circuit subsystem controller to the subsystem within the complex electrical device further includes interconnecting the subsystem with the additional electronic interface.

EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

None.